Birch Stewart Kolasch Birch LLP

Protecting the Product of your Mind®

Discussion of 35 U.S.C. § 103 Rejection and "Known Technique" Rationale

Intel Corporation v. PACT XPP Technologies AG
(Fed. Cir. 2023)

By: Eric H. Liou

Date: May 10, 2023

Overview

- Review 35 U.S.C. § 103 and Obviousness
- Supreme Court Decisions on Obviousness and "Known Technique" rationale
- IPR Proceeding of PACT's U.S. Patent 9,250,908
- *Intel Corporation v. PACT XPP Technologies* (Fed. Cir. 2023) - Decided: March 13, 2023
- Takeaways/Discussion of Federal Circuit Decision

35 U.S.C. § 103

- A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the **claimed invention as a whole** would have been **obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art** to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Graham v. John Deere Co. (U.S. Supreme Court: 1966)

- Obviousness is a question of law based on underlying factual inquiries.
- The factual inquiries include:
  - (A) Determining the scope and content of the prior art;
  - (B) Ascertaining the differences between the claimed invention and the prior art; and
  - (C) Resolving the level of ordinary skill in the pertinent art.
- Consideration of secondary considerations: evidence of commercial success, long-felt but unsolved needs, failure of others, and unexpected results.

KSR Int'l Co. v. Teleflex Inc. (U.S. Supreme Court: 2007)

KSR provided framework for supporting conclusions of obviousness with exemplary rationale:

- (A) Combining prior art elements according to known methods to yield predictable results;
- (B) Simple substitution of one known element for another to obtain predictable results;
- **(C) Use of known technique to improve similar devices (methods, or products) in the same way;**
- **(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;**
- (E) "Obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- (F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;
- (G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Statistics of 35 U.S.C. § 103 rejection

- 35 U.S.C. § 103 obviousness rejection is generally considered the most common rejection ground used by examiners at the U.S. Patent & Trademark Office to reject utility patent applications.
- Percentage of each rejection ground cited in Final Office Actions during period from 2005-2014* (*Note: more than one rejection ground can be cited in an Office Action*):
  - **35 U.S.C. § 103 rejection - 66%**
  - 35 U.S.C. § 102 rejection – 37.6%
  - 35 U.S.C. § 112 rejection – 22.1%
  - 35 U.S.C. § 101 rejection – 6.1%

* "Section 103 Rejections: How Common Are They and How Should You Respond?", available at: https://ipwatchdog.com/2016/10/03/103-rejections-common-respond/

Background – *Inter Partes* Review

- PACT XPP Technologies owns U.S. Patent 9,250,908 ('908 patent).
- Intel petitioned for *inter partes* review* (IPR) of independent claim 4 and dependent claim 5 of the '908 patent at the Patent Trial and Appeal Board (PTAB), asserting grounds of unpatentability based on obviousness.
  - PACT statutorily disclaimed claim 4 prior to PTAB's Final Written Decision.
  - Focus is on claim 5.
  - **At issue, theory of obviousness that relies upon combination of Kabemoto (U.S. Patent 5,890,217) and Bauman (U.S. Patent 5,680,571).**

*No. IPR2020-00518

Background – U.S. Patent 9,250,908

- Multi-processor Bus and Cache Interconnection System
- Assignee: PACT XPP Technologies, AG
- Technology is directed to multiprocessor systems and the access of stored data through a **main memory** (storing all of system's data) and various **cache memories** (storing smaller bits of same data).
- A system can use multiple cache levels, e.g., primary cache is closer to the processer and a secondary cache located away from processor.
- Use of multiple cache memories may cause problems for cache coherency**.**
- Different caches can have local copies of the same data; inconsistencies may arise if one processor changes its local copy of the data and that change is not propagated to the other copies of that data.
- To address problem, multiprocessor systems often require a mechanism to monitor and maintain cache coherency, e.g, shared entity to detect and make changes to all local data copies for consistency.

U.S. Patent 9,250,908 – Dependent Claim 5 at issue

- Includes limitations of independent claim 4 - focus on ***segment-to-segment*** limitation

4. *A system, the system comprising:*

a processing system comprising a plurality of processors; and

at least one separated cache not part [of] any processor;…,

wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors; the system further comprising:

an interconnect system interconnecting each of the separated cache segments with each of the processors, each of the processors with neighboring processors, and each of the separated cache segments with neighboring separated cache segments; *and*

an arbiter, the arbiter controlling access of a processor to the interconnect system.

Background – IPR of ’908 Patent

- Intel asserted that the prior art (U.S. Patent No. 5,890,217 to Kabemoto and U.S. Patent No. 5,680,571 to Bauman) teaches a *multiprocessor system that uses the separated cache and interconnect system* (***segment-to-segment* limitation**) according to claim 4 of ’908 patent.
- ***Segment-to-segment* limitation: “…***an interconnect system interconnecting…each of the separated cache segments with neighboring separated cache segments…”*

Prior Art – Kabemoto – Annotated FIGS. 3 and 4*

FIG. 3

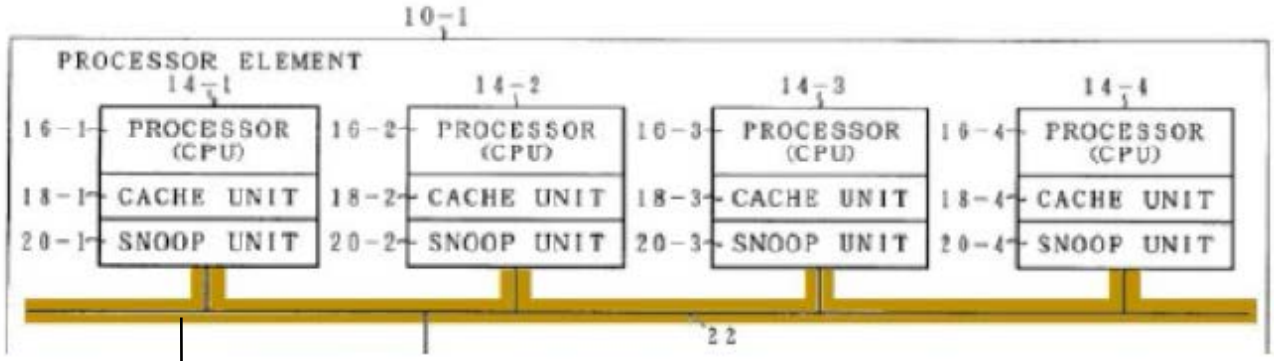
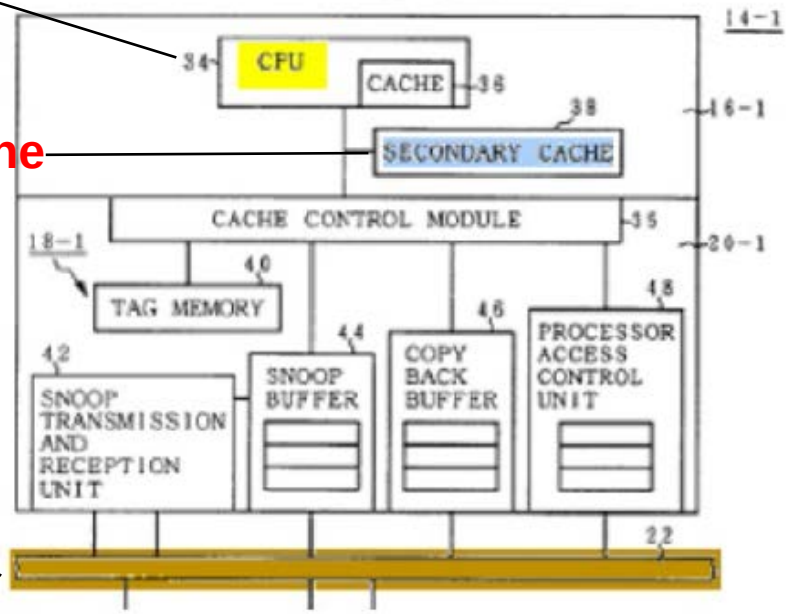


FIG. 4



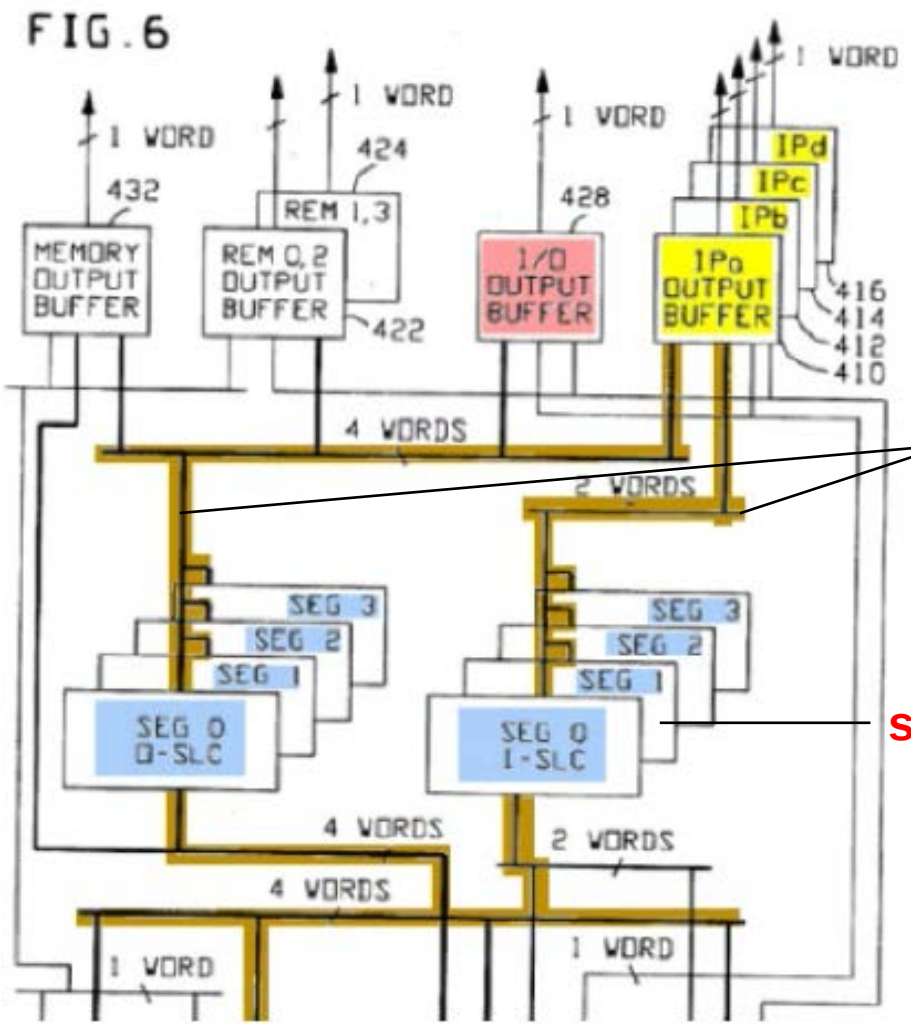
processor

secondary cache

Snoop bus (interconnection system)

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 5.

Prior Art – Bauman – Annotated FIG. 6*



interconnection system

segmented secondary cache

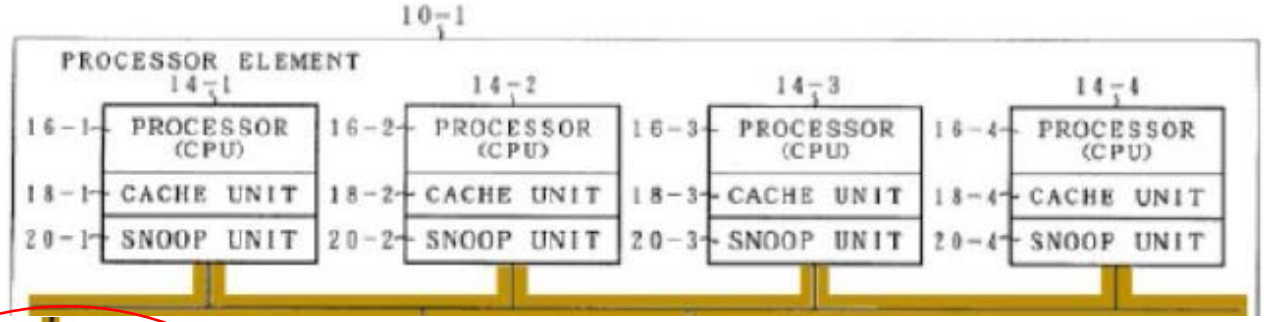
* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 6.

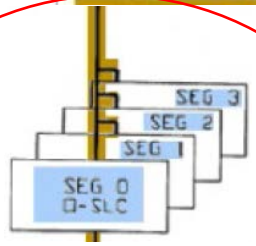
Background – Intel's Arguments in IPR of '908 Patent

- Intel's arguments for combination of Kabemoto and Bauman to teach claim 4:
  - Person of ordinary skill in the art would replace **Kabemoto's secondary caches** with **Bauman's global segmented secondary cache**.
  - Person of ordinary skill would connect Bauman's segmented secondary cache to Kabemoto's snoop bus 22 (interconnection system) on the outside of processor element 14-1 to reach a system with the claimed *separated cache and interconnect system* of '908 patent.

Intel's Proposed Combination of Kabemoto and Bauman's Systems

FIG. 3

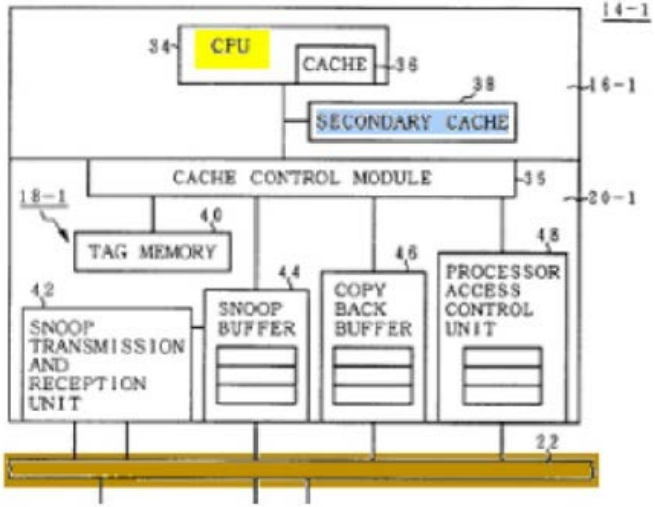




Bauman's segmented secondary cache

Kabemoto's processor elements

FIG. 4



Background – Intel's Arguments* in IPR of '908 Patent

- Intel relied on *KSR*'s "known technique" rational and asserted that *a person of ordinary skill would have been motivated to combine the teachings of Kabemoto and Bauman since they* "relate to the same field of multiprocessor . . . systems" and "address the same problem: maintaining cache coherency."
- "So, Intel reasoned, a person of ordinary skill 'would have naturally turned to Bauman's segmented [global secondary] cache to use . . . in Kabemoto' since Bauman's separated cache was known to address the same cache-coherency issue that Kabemoto also sought to address, just through a different mechanism—a shared snoop bus."

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 12.

Background – PACT's Arguments in IPR of '908 Patent

- PACT only argued that Intel failed to demonstrate a motivation to combine the teachings of Kabemoto and Bauman.
- No dispute that the combination of Kabemoto and Bauman taught each limitation of claim 4 of '908 patent (including the *segment-to-segment* limitation at issue).

IPR – PTAB's Decision of '908 Patent

- **PTAB Holding:**
  - **Since Intel failed to prove the obviousness of each limitation in claim 4, it upheld the patentability of claim 5.**
    - PTAB purported to "agree" with PACT that Intel failed to demonstrate the prior art disclosed the *segment-to-segment* limitation. *Note: PACT's counsel did not make this argument before the Board.*
  - **Concluded that Intel failed to show a person of ordinary skill in the art would have been motivated to combine the teachings of Kabemoto and Bauman.**

Background – PTAB's Reasoning* in IPR of '908 Patent

- PTAB concluded Intel did not establish *the segment-to-segment limitation* of claim 4 was disclosed in the prior art, since Intel failed to explain how Kabemoto's snoop bus 22 connected *each cache segment to its neighboring segment*.
- Considered this to be a "fatal flaw" since PTAB's understanding was that Intel relied on Kabemoto's snoop bus 22 to disclose all three limitations of the claimed "interconnect system" in the '908 patent.
  - Note: Intel relied on Bauman to teach *a separated and segmented cache* of claim 4 of '908 patent in its petition and the proceedings.
- PTAB rejected Intel's use of known-technique rationale and stated that "[i]f . . . Kabemoto already addresses [the] problem [of cache coherency] through the use of a known technique similar to that of Bauman's, [it] fail[ed] to see why one of ordinary skill in the art would regard Bauman's technique as an **obvious improvement** to Kabemoto."

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* pages 9 and 12.

IPR – PTAB's Decision of '908 Patent

- **PTAB holding: Since Intel failed to prove the obviousness of each limitation in claim 4, it upheld the patentability of claim 5.**

Appeal to Federal Circuit and Decision

- Before Circuit Judges NEWMAN, PROST and HUGHES
- Intel appealed the PTAB's Decision of upholding the patentability of claim 5 of '908 patent.

- ISSUE: Is there *substantial evidence* to support the PTAB's conclusions that the prior art fails to disclose the *segment-to-segment* limitation of claim 4 of the '908 patent AND a lack of motivation to combine the teachings of Kabemoto and Bauman?

Fed. Cir. – Std. of Review of PTAB's Decision

- **"Substantial Evidence Standard"** – directed to *such relevant evidence as a reasonable mind might accept as adequate to support a conclusion*. *AG v. Torrent Pharms. Ltd.*, 853 F.3d 1316, 1324 (Fed. Cir. 2017).
- "What the prior art discloses and whether a person of ordinary skill would have been motivated to combine prior art references" are both questions of fact that are reviewed for **substantial evidence**. *PAR Pharm., Inc. v. TWI Pharms., Inc*., 773 F.3d 1186, 1193 (Fed. Cir. 2014).

Fed. Cir. – Intel's Arguments on Appeal

- Intel argued PTAB's conclusions regarding '908 patent lack substantial evidence:

  (1) Substantial evidence does NOT support the Board's determination that the prior art fails to disclose the *segment-to-segment* limitation of claim 4; and

  (2) Substantial evidence does NOT support the Board's determination that there was no motivation to combine the teachings of Kabemoto and Bauman.

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* pgs. 7-8.

Summary of Intel's Arguments and Fed. Cir. Decision

- (1) PTAB's determination that the prior art fails to disclose the *segment-to-segment* limitation of claim 4:
  - Intel asserts FIG. 6 of Bauman teaches the *segment-to-segment* limitation.
  - **Fed. Cir. agrees with Intel and concludes that the PTAB's determination that the *segment-to-segment* limitation is NOT disclosed in the prior art lacks substantial evidence.**
- (2) PTAB's determination that there was no motivation to combine the teachings of Kabemoto and Bauman.
  - Intel argues that the PTAB's rejection of its "known-technique" rationale for a motivation to combine the teachings of Kabemoto and Bauman lacks substantial evidence.
  - **Fed. Cir. agrees with Intel and reverses the PTAB's determination (e.g., motivation to combine Kabemoto and Bauman exists).**

Fed. Cir. – Analysis/Reasoning

(1) Review of PTAB's determination that the prior art fails to disclose the *segment-to-segment* limitation of claim 4:

FIG. 6 and col. 11, lines 18-26 of Bauman:

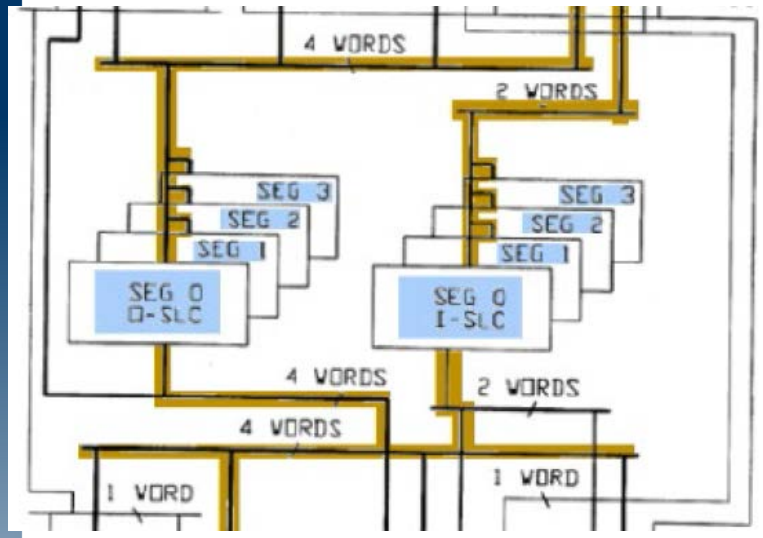


FIG. **6** is a block diagram that illustrates the data path between the requesting processors, the second-level cache, and the memory. Segments **0-3** of the operand second-level cache and Segments **0-3** of the instruction second-level cache are shared between the **I/O** Subsystem, IPa, IPb, IPc, IPd, and the remote Address ASIC. There is also an access path to and from the Memory Subsystem (**1** or **2**). The data to and from these requesters is structured as separate read and write interfaces.

Fed. Cir. stated, "*Bauman's Figure 6 teaches—if not plainly illustrates— the segment-to-segment limitation of the claimed interconnect system: each blue cache segment is connected to its neighboring blue cache segments via the gold data path*."*

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 9.

Fed. Cir. – Legal Principles on Obviousness and Analysis

- (2) Review of PTAB's determination that there was no motivation to combine ("known-technique" rationale) the teachings of Kabemoto and Bauman:
- **Prior Case Law: *KSR vs. Teleflex*:**
  - "[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed."
  - Motivation to combine analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ."
- **Prior Case Law: *Intel Corp. Vs. Qualcomm Inc. 21 F.4th 784* (Fed. Cir. 2021):**
  - Fed. Cir. previously stated "universal" motivations known in a particular field to improve technology provide "a motivation to combine prior art references <u>even absent any hint of suggestion in the references themselves</u>."
    - Board's rejection of "increasing energy efficiency" as a "generic concern" in electronics as a motivation to combine references lacked substantial evidence.

Fed. Cir. – Review of Legal Principles on "Known Technique" Rationale for Motivation to Combine Prior Art References

- ***KSR vs. Teleflex*:**
  - "…if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill."
  - Assessing whether claimed subject matter involves the "application of a known technique" will "[o]ften" require "a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art."
- ***Intel Corp. Vs. Qualcomm* (Fed. Cir. 2021):**
  - "if there's a **known technique to address a known problem** using 'prior art elements according to their **established functions**,' then there is a motivation to combine."
  - To address a known problem, "[i]t's not necessary to show that a combination is the best option, only that it be a **suitable option**."

Fed. Cir. – Analysis of PTAB's Decision

(2) Review of PTAB's determination that there was no motivation to combine the teachings of Kabemoto and Bauman using the "known-technique" rationale:

- Intel's assertion: A person of ordinary skill would have been motivated to combine Kabemoto and Bauman since they are directed to the **same field** (multiprocessor systems) and **same problem** (maintaining cache coherency).
- PTAB's conclusion: Kabemoto already addresses the *cache coherency* issue (with a technique similar to Bauman's technique), and it is unclear why one of ordinary skill in the art would regard Bauman's technique as an **obvious improvement** to Kabemoto.
- Fed. Cir.: "Kabemoto and Bauman address the same problem and that Bauman's cache was a known way to address that problem is precisely the reason that there's a motivation to combine under KSR and our precedent."*
  - ***KSR* and *Intel* cases: motivation to combine exists when a known technique "has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way" using "prior art elements according to their established functions".**

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 12.

Fed. Cir. – Analysis of PTAB's Decision

- Fed. Cir. noted no disputes with respect to:
  - Bauman's *global segmented secondary cache* for improving cache coherency in multiprocessor systems, and recognition by a person of ordinary skill that such cache would improve other similar multiprocessor systems as in Kabemoto, by addressing the same cache coherency problem; and
  - the asserted combination that would be a use of Bauman's secondary cache "according to [its] established function".
- Contrary to the PTAB's suggestion, Fed. Cir. stated there was no requirement for Intel to show that replacing Kabemoto's secondary cache with Bauman's secondary cache was an "**improvement**"; it was sufficient for Intel to show Bauman's secondary cache was a "**suitable option**" to replace Kabemoto's secondary cache to establish obviousness.
- **Fed. Cir. stated, "It's enough for Intel to show that there was a known problem of cache coherency in the art, that Bauman's secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn't beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under KSR…"*, and reversed PTAB's decision.**

* Fed. Cir. Opinion - *Intel Corp. v. PACT XPP Technologies,* page 13.

Fed Cir. - Decision

- Fed. Cir reversed: (1) PTAB's determination that the prior art fails to disclose the *segment-to-segment* limitation of independent claim 4; and (2) PTAB's determination that there was no motivation to combine the teachings of Kabemoto and Bauman.
- Fed. Cir. remanded the case back to PTAB to address any remaining dispute on the patentability of dependent claim 5.
  - Intel relied upon prior art to teach limitations of claim 5, but PTAB did not analyze claim 5 as a whole.

Thank you.

Questions?

eliou@bskb.com